



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/699,707

11/03/2003

Antonio F. Mondragon-Torres

TI-35731

3525

23494 7590 05/29/2008
TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER

LEE, SIU M

ART UNIT

PAPER NUMBER

2611

NOTIFICATION DATE

DELIVERY MODE

05/29/2008

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com
uspto@dlemail.itg.ti.com

Office Action Summary	Application No. 10/699,707	Applicant(s) MONDRAGON-TORRES ET AL.	
	Examiner SIU M. LEE	Art Unit 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 February 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 3-9, 11-16 and 18-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 3-9, 11, 12, 16 and 18-22 is/are rejected.
- 7) ☒ Claim(s) 13-15 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 November 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 3-9, 11-16, 18-22 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the first control mechanism, the second control mechanism, and the third control mechanism must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Art Unit: 2611

Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 5-9, 18-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

- (1) Regarding claims 5 and 8:

Claim 5 recites “a first control mechanism, a second control mechanism, and a third control mechanism” for configuring an adaptive equalizer. Figure 6a – 6e disclose the equalizer after the configuration, but none of the control mechanism is disclosed in the specification or the drawing.

- (2) Regarding claim 18:

Claim 18 recites "a means for configuring the two or more adaptive equalizers and the plurality of operational blocks according to attributes of a signal profile". None of these means are disclosed in the specification or the drawing.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda (US 5,644,59) in view of Suzuki et al. (US 2003/0133493 A1).

(1) Regarding claim 11:

Ueda discloses receiving a multi-path signal profile (abstract, lines 2-4); determining attributes of the multi-path signal profile (a plurality of delay measuring circuits each supplied with each detected signal as input and for detecting a multi-path propagation characteristics of a channel, column 14, lines 47-50); and operating two or more adaptive equalizers, computational resources of the two or more adaptive equalizers, and operational blocks interconnecting said two or more adaptive equalizers according to said attributes of the multi-path signal profile (means for selecting one of the equalized outputs produced from the plurality of decision feedback adaptive equalizers or one of equalized outputs produced from the plurality of linear adaptive equalizers based on the results measured by the delay measuring circuits and setting

the selected one equalized output as a final equalized output, whereby the adaptive equalizers which are expected to show better performance than that of the other with respect to the multi-path propagation characteristics measured by the respective delay measuring circuits, are activated every branches to thereby produce equalized outputs for every branches and characteristics of the equalized outputs produced every branches are thereafter compared to thereby set the output of the adaptive equalizer which is best in equalization characteristic as a final equalized output from the result of comparison, column 14, lines 50-65).

Ueda fails to disclose the determining comprises determining a number of antennas at a transmitter.

However, Suzuki discloses a path search portion in figure 8 that shows the process of the generating the power delay profile. The remove of modifying component 23 separate the received signal into signals from different transmitting antenna A1 and A2, and then through power averaging 251 and 252 and generating delay profiles for each antenna in 26 and combining the two delay profiles from each antenna in block 27 to generate the delay profile (paragraph 0010 and paragraph 0073-0074).

It is desirable to determine a number of antennas at a transmitter before generation the power delay profile because the estimation depends on the number of antenna in the transmitter to correctly generate the power delay profile. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Suzuki in the system of Ueda to improve the accuracy of the power delay profile.

(2) Regarding claim 16:

Ueda further discloses that disabling at least one selected from the group: adaptive equalizer; operational block; and computational resource (the performance of the plurality of decision feedback adaptive equalizers and those of the plurality of linear adaptive equalizers are respectively compared to thereby set the output of one of the adaptive equalizers, which is best in equalization characteristic, as a final equalized output from the result of comparison, and the remaining adaptive equalizers are deactivated, column 12, lines 41-48).

7. Claims 18-20, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda (US 5,644,597) in view of Master et al. (US 7,320,062 B2).

(1) Regarding claim 18:

Regarding claim 17 (the examiner interpreted “the signal profile” as “a signal profile” in line 7 of claim 17):

Ueda discloses a system comprising two or more adaptive equalizers (adaptive equalizer 127, 130, 133, 136 in figure 11); a plurality of operational blocks (received-signal memory 110 and 117 and square error integrated circuits 128, 131, 134, 137, equalized-output memory 129, 132, 135, 138 and comparator 139, and selecting circuit 140 in figure 11); means for selectively interconnecting the two or more adaptive equalizers and the plurality of operational blocks (the comparator 139 compares the results outputted from the equalized square error integrating circuit 128, the equalized square error integrating circuit 131, the equalized square error integrating circuit 134

Art Unit: 2611

and the equalized square error integrating circuit 137. Next, the comparator 139 selects the adaptive equalizer that is expected to have the minimum sum of equalized square errors, i.e., to have the best performance with respect to its burst. Thereafter, the comparator 139 outputs the result of selection to the selecting circuit 140 and outputs a stop signal to each of the remaining three adaptive equalizers that have not been selected. These adaptive equalizers stop the equalization of the remaining random data corresponding to the same burst in response to the stop signal, column 36, lines 6-19); and means for configuring the two or more adaptive equalizers and operational blocks according to attributes of the signal profile (the decision feedback adaptive equalizer which shows excellent performance under frequency selective fading in which a delay time interval of a delay wave is long and the linear adaptive equalizer which shows excellent performance under frequency selective fading in which a delay time interval of a delay wave is short and fading in which a delay wave does not exist, therefore, when the comparator 172 compares the square error values of each adaptive equalizer, it is comparing according to the signal profile of the incoming signal and from the comparison, decide which adaptive equalizer to use and which adaptive equalizer to deactivate, column 15, lines 16-23, the comparator 172 compares the sum of squared error values SE12, SE22, SE32, SE42 and selection signal to the equalized-output memory 161, 164, 167, 170 and configure the equalizers and equalized output memory so that a selected signal will be output in the terminal 126, figure 13, column 45, lines 5-51).

Ueda fails to disclose means for selectively interconnecting the two or more adaptive equalizer and the plurality of operational blocks, the means for selectively interconnecting comprises a plurality of multiplexers.

However, Master discloses a interconnection that comprises a plurality of multiplexers (multiplexers 280 in figure 6) for connecting a plurality of operational blocks (computational elements 250A) and is control by a control bits 265 for activating or deactivating input enables, input selects, output selects, mux selects, demux enables, demux selects, and demux output selects (column 19, lines 13-21).

It is desirable to have means for selectively interconnecting the two or more adaptive equalizer and the plurality of operational blocks, the means for selectively interconnecting comprises a plurality of multiplexers because of low power and low complexity. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Master in the system of Ueda to provide a simple and low power consumption system.

(2) Regarding claim 19:

Ueda discloses the system comprises means for disabling at least one of the pluralities of operational blocks according to said attributes of the signal profile (the comparator 172 outputs a stop signal to each of the remaining three adaptive equalizers which have not been selected, column 36, lines 13-17).

(3) Regarding claim 20:

Ueda discloses the system comprises means for disabling a computational resource of at least one of the two or more adaptive equalizers according to said

attributes of the signal profile (the comparator 172 outputs a stop signal to each of the remaining three adaptive equalizers which have not been selected, column 36, lines 13-17).

(4) Regarding claim 22:

Ueda discloses the system wherein the attributes of the signal profile comprise at least one selected from the group consisting of: a number of antennas that transmitted the multi-path signal; a length of the multi-path signal profile; an amount of energy in a single sub-signal of the multi-path signal; an amount of capturable energy by a number of adaptive equalizers; and a number of energy clusters (Ueda discloses the attributes of the signal profile comprises a length of the multi-path signal profile, there is a method of activating the linear adaptive equalizer 176 if the maximum delay time of the delay wave is less than or equal to 0.35 symbol and of activating the decision feedback adaptive equalizer 175 if the maximum delay time is more than or equal to 0.35 symbol, column 46, line 64 – column 47, line 2).

8. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda (US 5,644,597) in view of Master et al. (US 7,320,062 B2) as applied to claim 18 above, and further in view of Juan (US 5,642,382).

Ueda and Master disclose all the subject matter as discussed in claim 18 except the system further comprising means for sharing computational resources of the two or more adaptive equalizers.

However, Juan discloses a system that share a single set of arithmetic operators between filters of the equalizers (column 2, lines 4-10).

It is desirable to share computational resources of the two or more adaptive equalizers because it can reduce hardware requirement and lower production cost (column 2, lines 4). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the teaching of Juan in the system of Ueda and Master to lower the production cost.

9. Claims 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda (US 5,644,597) in view of Suzuki et al. (US 2003/0133493 A1) as applied to claim 11 above, and further in view of Terao (US 7,039,097 B2).

Ueda and Suzuki disclose all the subject matter as discussed in claim 11 and further discloses the number of antenna except wherein determining attributes of the multi-path signal profile comprises determining a delay length of the multi-path signal profile if said number of antenna is equal to one.

However, Terao discloses a delay profile measuring unit 33 that calculates delay profile as a function of delay of the received signal (it is inherent that the number of transmitting antenna has at least one antenna) (column 6, lines 14-19).

It is desirable to calculate the delay profile as a function of delay because it can reduce the amount of calculation and power consumption. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to employ the

Art Unit: 2611

teaching of Terao in the method of Ueda and Suzuki to improve the efficiency of the method.

Allowable Subject Matter

10. Claims 13-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Liang et al. (US 2003/0133424 A1) discloses a path diversity equalization CDMA downlink receiver.

Yang (US 6,763,074 B1) discloses an adaptive configurable demodulation system with multiple operating modes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SIU M. LEE whose telephone number is (571)270-1083. The examiner can normally be reached on Mon-Fri, 7:30-4:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Siu M Lee/
Examiner, Art Unit 2611
5/21/2008

/CHIEH M FAN/
Supervisory Patent Examiner, Art Unit 2611